Amendments to the Claims

The current listing of the claims replaces all previous amendments and listings of the claims.

Claim 1 (Currently Amended): An image processor comprising:

a switch configured to divide image data into m x n pixels, having n lines with m pixels per one line and to transfer ~~without storing in the switch~~ each one of the n lines of image data to a predetermined destination;

a storage unit including (n-1) number of memories each configured to store one line of the n lines of the image data;

a control unit configured to control the transfer of the each one of the n lines of the image data to the predetermined destination;

a compression unit configured to batch compress the image data of m x n pixels,

wherein said control unit is further configured to control said switch to directly transfer (n-1) lines of the n lines of the image data to the (n-1) number of memories, and a remaining one line of the n lines of the image data directly to said compression unit; and to control the storage unit to transfer the (n-1) lines of the image data stored in the (n-1) number of memories to said compression unit.

Claim 2 (Previously Presented): The image processor according to claim 1, wherein the (n-1) number of memories are (n-1) number of FIFO (first-in first-out) memories.

Claims 3-5 (Canceled)

Claim 6 (Currently Amended): An image processor comprising:

means for dividing image data into m x n pixels, having n lines with m pixels per one line;

means for transferring without storing in the means for transferring each one of n lines of the image data to a predetermined destination;

means for switching the predetermined destination for the each one of the n lines of the image data;

means for storing (n-1) lines of the image data;

means for controlling the transfer of each one of the n lines of the image data to the predetermined destination;

means for batch compressing the image data of m x n pixels,

wherein said means for controlling controls said means for switching to directly transfer ~~without storing~~ (n-1) lines of the n lines of the image data to said means for storing, and the remaining one line of the n lines of the image data directly to said means for batch compressing; and controls the means for storing to transfer the (n-1) lines of the image data stored in the means for storing to said means for batch compressing.

Claim 7 (Previously Presented): The image processor according to claim 6, wherein said means for storing comprises (n-1) number of FIFO (first-in first-out) memories.

Claims 8-10 (Canceled)

Claim 11 (Currently Amended): An image processing method comprising:

dividing image data into m x n pixels, having n lines with m pixels per one line;

transferring ~~without storing~~ each one of the n lines of the image data to a predetermined destination;

switching the predetermined destination for the each one of the n lines of the image data;

storing one line of the n lines of the image data in each of (n-1) number of memories;

batch compressing the image data of m x n pixels,

wherein said transferring directly transfers (n-1) lines of the n lines of the image data to said (n-1) number of memories and the remaining one line of the n lines of the image data directly to a compression unit based on said switching; and transfers the (n-1) lines stored in the (n-1) number of memories to said compression unit.

Claims 12 and 13 (Canceled)